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## Introduction

The GEKCO video pattern generator is a versatile instrument for testing a wide range of video processing and display applications. Please refer to the companion document, *A Video Tutorial*, which describes in detail, a review of color video and why do we need a video test pattern generator and what each test pattern is used for .

This unit generates all the major video test patterns needed for video system evaluation and test. The VG10 provides the following:

## Features

- 9-bit digital signal processing generation.
- Simultaneous Composite and Y/C (S-Video) outputs
- Standard BNC and 4 Pin Mini Din S-Video Connectors
- AC or DC power supply.

### Configuration Options

#### Basic Version Model VG10

- NTSC Color Black

#### Standard Version Model VG10-STD

- SMPTE Color Bars with pluge
- Color Black 7.5 IRE setup output.
- Video Standard NTSC (RS170A)

#### Multiple Test Patterns Model VG10-OPT1

- SMPTE Color Bars with pluge
- Color Black with 7.5 IRE setup
- Full field Color Bars 100.75
- Full Field EIA Color Bars 75.75
- Red Field
- Green Field
- Blue Field
- White Window
- Pattern selection saved during power off

#### Enhanced Test Patterns VG10-OPT2

- Multiburst
- Cable Sweep with markers
- 5 Step Stair Case
- 10 Step Stair Case
- Modulated Ramp
- Cross Hatch
- Center Cross with Safe Area
- Bounce
- Test Signal Matrix

#### Character Identification Display VG10-OSD Option 3

- On screen display with 12 character changeable text.
- Characters and setup is preserved during power down.

#### Audio T VG10-A

#### Audio Tone Output VG10-AUD Option 4

- 1 kHz Audio Test Tone Output, Odbm nominal output level (adjustable)

The VG10 is housed in a compact, rugged mechanical package and with AC/DC power operation, is suitable for studio, mobile unit and field portable applications.

The separate AC to DC power transformer is included in any version. A optional battery power pack is available.

A rack mount option is also available

**Electrical Characteristics****Test Signal Generator**

Luminance Accuracy less than 5%.

Hue Accuracy less than 2.5 degrees.

Color Saturation Accuracy less than 2%.

Differential Gain less than 2.5 degrees.

Burst Frequency Error +/- 100 Hz of Standard  
(NTSC 3.579545 MHz)

**Video Outputs**

S-Video Connector (1) 4-pin mini-DIN.

Standards NTSC RS170A

**Audio Output**

Connector: XLR male balanced

Frequency 1 kHz

Amplitude: 0 to +8dBu into 600 ohm or a high  
impedance load.

**Power Source**

AC Adapter 110 VAC to 9VDC.

External 9-12VDC less than 300mA.

**Environmental****Temperature**

Operating 0C to +35C

Nonoperating -40C to +65C

**Physical Characteristics**

<b>Dimensions</b>	<b>mm</b>	<b>in.</b>
Width	137	5.4"
Height	39	1.5"
Depth	178	7.0"
<b>Weight</b>	<b>kg</b>	<b>lbs</b>
Net	0.48	1.06
Shipping	1.5	3.31

**GEKCO reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate features in products previously sold.**

# Operation

## Video Pattern Selection

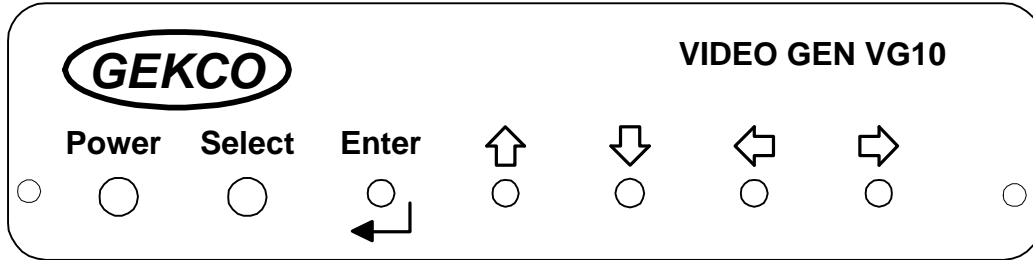


Figure 1. Front Panel

### Front Panel Control

The Front Panel allows selection of the desired test pattern and on screen display control.

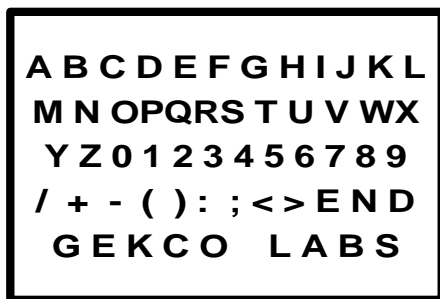
### Pattern Selection

The **↑ (up)** and **↓ (down)** buttons are used to control the pattern selection. If the enhanced patterns are available the **left** and **right** buttons are used to page to the next page of patterns. Press the **↑ (up)** arrow button to select patterns in sequential order or down to reverse the selection ordering. Patterns will change while the switch is pressed or step through them one at a time for each key press. Un press the switch to halt the pattern sequencing. If no changes were made after 4 seconds the current pattern setup will be stored to non-volatile memory for later recall on power up.

### On Screen Display (OSD) Control

The OSD text message can be up to 12 characters long, 8 different colors, black block or shadow outline, and movable text position.

The arrow buttons, **up**, **down**, **left** and **right** are used to setup the OSD. The **“Enter”** button is used in a dual purpose mode depending on the time that it is held pressed. A short press turns on or off the OSD character display. A long press, about 2 seconds will start the OSD selection mode. The OSD display menu will appear with the alphabet displayed and the selected character will be blinking.



Use the **up**, **down**, **left** and **right** control buttons to chose the appropriate character. The control button can be held down to sequence the move at a 1 character per second rate. Push the **“Enter”** button to select the character. The selected character will be shown on the display line

where the box was blinking and the blinking box will move to the next position waiting for the selection of another character.

The display line can be created in this manner up to 12 characters. To *backspace* select the left arrow icon on the menu and to add a *space* select the right arrow icon.

The background and color of the characters in text message is adjustable. The background can either be a black block outline or a black shadow outline. Move the selection cursor to any characters on the menu that spell “**BKGRND**”. Push the “**Enter**” button to toggle the background mode.

The character color can be selected in a similar manor. Select any characters on the menu that spell “**COLOR**”. Push the “**Enter**” button to sequence through the colors. The colors available are, Gray, Magenta, Cyan, Blue, Yellow, Red, Green and Black. The colors will sequence through the list and repeat.

To exit any selection mode move the blinking cursor to the word “**END**” and press **Enter**. This will display and allow movement of the text message. Use the arrow keys to position the display as desired. Press **Enter** again to exit the OSD menu and return to normal operation. All the OSD parameters are stored to non-volatile memory for recall on power up.

The OSD Display can be turned On or Off. If it is not desired press **Enter** until the text display disappears and then it can be turned on again after a 2 second wait by pressing Enter again until the display re-appears.

### ***Configuration Control***

The Configuration Control dip switch is used to configure the unit for NTSC or PAL format video and to enable the test diagnostics on power up. (*Available in future versions*)

## **Service Information**

This unit uses digital signal processing so there is little need for adjustment. The only adjustments that may be required are Output Video and Audio level adjustments.

### ***Calibration***

#### Output Video Level Adjustment

Terminate the composite video output into a 75 ohm load and measure the video output level using the SMPTE bar pattern. Adjust R35 for a 1V p-p output level.

#### Output Audio Level Adjustment

Terminate the audio output into a 600 ohm load and adjust R25 for 0 dBu (.775 VAC rms) output level.



# Theory of Operation

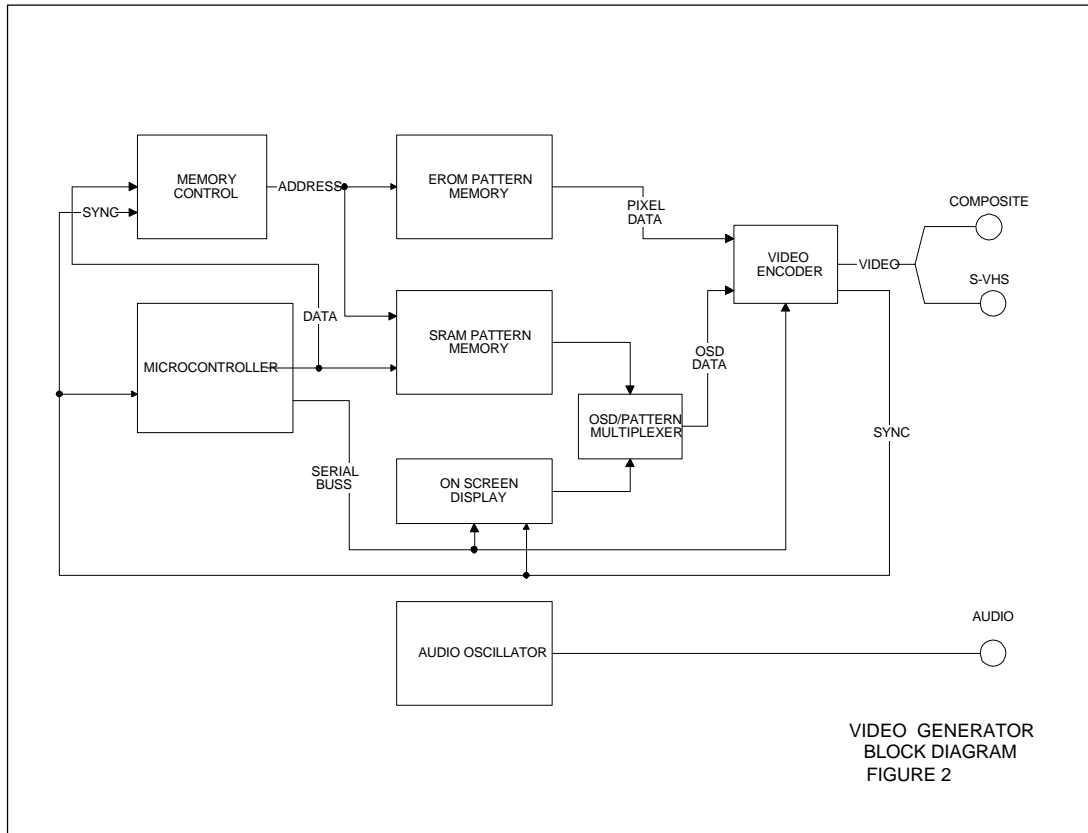


Figure 2. Block Diagram

Refer to Figure 2 for the following discussion:

The video pattern generator creates the composite video waveforms, described in the companion document, *A Video Tutorial*, with the following functional blocks.

The functional blocks are from back to front, Video Encoder, SRAM Pattern Memory, Eprom Pattern Memory, On Screen Display, Memory Control, and the Microcontroller.

Let's start from the back end and work forward in our detail discussion of how this unit works. The Composite Video and S-VHS outputs are generated by the Video Encoder.

The Video Encoder generates the analog video from digital data from one of two input ports. The two ports are called Pixel Data and On Screen Display data or OSD for short. These two data streams come from the Pattern Memory.

The Pattern Memory stores the digital information to create the waveform and presents the data to the Encoder. This design has two sources of Pattern Memory, Static Random Access Memory (SRAM) and Electrically Programmable Read Only (EPROM) Memory.

The Memory control and Microcontroller use the sync signal from the Encoder for timing information and control the Pattern Memory to provide the digital data to the Video Encoder at the proper time.

## **Hardware**

### **Video Encoder**

The Video Encoder has a number of built in functions, a sync generator, digital signal processing and the digital to analog conversion to create the composite video waveform. The sync signals are created in the encoder and the video waveforms can come into two ports, a pixel data port and a on screen display (OSD) port. One bit on the OSD port determines which port is used and can be dynamically switched. The encoder block adds sync information to the selected input port data and creates the composite video waveform. The combined digital signal is converted to analog and adjustable on the output. Since the encoder generates the sync signals it is the master timing source for the pattern generator.

### **Sync Generation**

The Encoder is programmed to generate Vertical and Horizontal Sync, and Composite Blanking for the Microcontroller, Memory Control functions and On Screen Display. A IIC bus is used to program the encoder by the Microcontroller.

### **Digital to Analog Conversion**

The Encoder has three D to A converters. One for the Composite Video, Luminance (Y) and Chrominance (C). The digital input data is 2 times over sampled and converted to analog at a clock rate of 27 MHz.

### **Output Video Filtering**

Since the video encoder generates analog signals from a digital source the analog output contains digital samples or discrete steps. The analog filters on the output smooth out the discrete steps.

## Control Functions

### *Microcontroller*

The micro controller's function is to initialize the peripherals, load the static ram display memory, and actively control the line pattern to create the test pattern.

The microcontroller has the following jobs:

1. Dynamically select the proper video pattern line to display
2. Create the video line pattern and store in static ram memory.
3. Monitor the front panel switches for pattern control and OSD creation and control.
4. Initialize and program the video encoder
5. Initialize the On Screen Display

### *Front Panel Interface*

The Front Panel switches are read by the microcontroller on the data bus by a bus transceiver. The switches allow pattern selection and On Screen Display control.

The Configuration Dip Switch allows for video format selection and test diagnostics enable. The video format can either be NTSC or PAL. If the test bit is selected on the dip switch the internal diagnostics test is ran during initialization. Normally this should be off to reduce the start up time.

### *Memory and OSD Control*

The Memory and OSD Control block perform the pixel memory address generation , pixel clock division and OSD data control.

## Video Pattern Generation

There are two sources of the pattern image. One for the OSD port and one for the pixel port. The video encoder either converts the OSD port or the pixel data port to analog video with sync.

### *OSD Port*

The On Screen Display (OSD) port memory is a smaller memory for less complicated patterns.

### *Pixel Port Memory*

The pixel port memory is used for the more complicated higher resolution video patterns. The pixel data rate is twice the rate of the OSD port and the data width is much greater so it takes more memory.

## Character Generation

The On Screen Display (OSD) is a stand alone character generator. The OSD receives synchronizing information from the Encoder and generates the video pattern and the proper timing to display previously created character text strings.

## Audio Generation

The audio source is created by a wein bridge 1 kHz oscillator. A dual op amp driver is used for balanced audio output.

### **Power Supply**

Power to the unit is available through a external AC to DC plug in transformer. 9 to 12 VDC is required at the power connector. A internal regulator powers the main circuitry and the audio section has a negative supply provided by a simple switching supply circuit.

## Software

### Memory Map

Table 1. Microprocessor Port Assignments

I/O PORTS	DATA DIR	FUNCTION
PA0 > A0	OUT	REGISTER DECODE 0
PA1 > A1	OUT	REGISTER DECODE 1
PA2 > A2	OUT	CHIP SELECT DECODE 0
PA3 > A3	OUT	CHIP SELECT DECODE 1
PA4 > A4	OUT	CHIP SELECT DECODE 2
PA5 > /DBMEN	OUT	BUS XCVR LOW ENABLE /CS0
PA6 > R/W	OUT	READ/WRITE
PA7 > /DS	OUT	DATA STROBE
PB5 > SDO	OUT	SERIAL DATA OUT
PB6 > SDI	IN	SERIAL DATA IN
PB7 > SCK	OUT	SERIAL CLOCK
PC0 > D0	BI	DATA BUS BIT 0
PC1 > D1	BI	DATA BUS BIT 1
PC2 > D2	BI	DATA BUS BIT 2
PC3 > D3	BI	DATA BUS BIT 3
PC4 > D4	BI	DATA BUS BIT 4
PC5 > D5	BI	DATA BUS BIT 5
PC6 > D6	BI	DATA BUS BIT 6
PC7 > D7	BI	DATA BUS BIT 7
PD5 > D5	IN	
PD7 > TCAP	IN	

Table 2. Address Decoder Assignments

A4	A3	A2	A1	A0	OUTPUT	MNEUMONIC FUNCTION
0	0	0	X	X	/CS0	DIP SWITCH ENABLE
0	0	1	X	X	/CS1	SRAM MEMORY DATA BUS OUTPUT ENABLE
0	1	0	X	X	/CS2	EPROM MEMORY DATA BUS OUTPUT ENABLE
0	1	1	X	X	/CS3	MEMORY CONTROLLER CHIP SELECT
0	1	1	0	0	LB_LD	ADR COUNTER LOW BYTE LOAD
0	1	1	0	1	HB_LD	ADR COUNTER HIGH BYTE LOAD
0	1	1	1	0	LINEREG	LINE ADDRESS REGISTER
0	1	1	1	1	UNUSED	SPARE
1	0	0	X	X	/CS4	OSD /CS
1	0	1	X	X	CS5	SERIAL EEPROM CS "ACTIVE HIGH"
1	1	0	X	X	/LEDCOM	LED COMMON
1	1	1	X	X	DESELECT	USED TO DISABLE ALL PERIPHERALS

## Software Outline

### *Initialization*

- Initialize Data Ports
- Run Diagnostics if switch is set.
  - Check Memory
    - If memory tests OK turn on "Select" LED for 1 second
- Load the Encoder Look Up Table
- Initialize the Encoder
- Initialize the On Screen Display
- Load Memory with patterns
- Enable Memory Control logic
- Enable interrupts

### *Pattern Generation*

#### MAIN ROUTINE

The main routine reads the front panel switch value in memory and then looks through the frame pattern lookup table to set the line address accordingly. The horizontal lines are counted to keep track of which line we are generating to address the pattern memory accordingly. Horizontal sync from the encoder is used for counting horizontal lines.

### *Interrupt Processing*

The external interrupt is caused by vertical sync from the encoder.

The external interrupt routine reads the front panel switch and stores to memory for later use. It also clears "LINECNT" variable which is used to count horizontal lines for the line pattern memory address generation.

## Circuit Description

Figure 3. Detailed Block Diagram

## ***Encoder***

The Brooktree BT866 Composite Video Encoder, U14, is used to generate analog composite video and Y/C (S-Video) from a digital 16 bit data stream or a 4 bit OSD input. The BT866 also generates the sync timing signals necessary for the composite video and control sections of the design. For more detailed information on the encoder refer to the BT866 data sheet from Brooktree.

## **Pixel Input Bus**

The pixel digital data is 24 bits wide. 8 bits are for luminance and 8 bits each of color difference data. The enhanced pattern memory data is connected to this bus.

## **On Screen Display Bus**

The OSD port input is the 4 bit address for a look up table to create a 24 bit digital value. This look up table is initialized on power up and is used for the less complicated patterns in this design and the On Screen Display.

## **Analog Outputs**

There are three analog outputs. One for composites video and two for S-VHS video. The luminance Y channel and chrominance C channel.

## **Output Filter Networks**

A three-pole elliptic filter (1 inductor, 3 capacitors) with a 6.75MHz passband is used to provide at least 45 dB attenuation (including  $\sin x/x$  loss) of frequency components above 20 MHz. There is one filter network for each analog output, composite video and the S-video luminance Y and chrominance C channel.

## ***Memory Control Logic***

The control logic used in the design is implemented with Lattice in circuit programmable logic. The logic is separated into two functions. One is Address Control and every thing else is titled Miscellaneous Control. Each logic block is implemented in a Lattice 2032 Electrically Erasable Programmable Logic Device (EEPLD).

## **Memory Address Control**

The Address Controller allows the micro controller to control the address bus during power up initialization and then during normal mode the address bits are a counter of the pixel clock. Bits 0 through 8 are outputs of a pixel counter and the high order bits 9 to 14 are controlled by the micro controller to select which line pattern is displayed during that line.

## **OSD/Pattern Multiplexing**

The Miscellaneous Control block has the following functions. A fixed pixel counter pre-scalar, a mux to allow control logic to be selected during initialization and the demultiplexer to separate the 8 bit byte to two 4 bit nibbles with another mux to select either OSD data or pixel display pattern data.



## ***Pattern Memory***

### **Static Ram Memory**

The pattern memory, U9, is a 8k by 8 Static Ram for the standard option and 32k by 8 Static Ram for the multiple pattern option. The memory is organized as 16 or 64 lines of 512 pixels by 4 bits per pixel. During the initialization sequence the pixel patterns stored in the micro controller are transferred to the static ram. Once initialization is complete the address control logic controls the address bus to generate the pixel pattern necessary for the specific display pattern.

### **EPROM Memory**

The Pattern Eproms, U7 and U8, are used to generate special patterns needed for extra test functions. The memory is organized as two banks of 32k x 8. One bank is used for the Luminance, U7 and one for the Chrominance channel, U8. Each memory bank has 32 lines of 1024 pixels. Only 720 pixels per line are used in this design.

### **Bus Transceiver**

The Bus Transceiver, U2, is used to allow the micro controller to take over the pixel bus and read and write data to the static ram. The address decoder is used to control the enable and bus direction on the transceiver.

## ***Microcontroller Logic***

Microcontroller Section

### **Microcontroller**

The microcontroller, U1, is a Motorola MC68HC705P9 multipurpose controller. The clock is divided by 8 from the 27 MHz system oscillator by U12, and enters the part on pin 27. The reset signal on pin1 is active low and controlled by U4. Multipurpose I/O PA0-PA7 are used for peripheral chip selects and memory control. PB5-7 are used for Serial Buss Communication and the IIC buss to communicate with the peripheral devices. PC0-7 are used for the data buss to load and read from SRAM memory. See the port assignments map for details.

### **Address Decoding**

The address decoder U5, a GAL16V8, decodes the address bits to create peripheral chip selects to enable different devices on the data bus. See the memory map in the software section for the address decoding map.

## **Front Panel Interface**

### ***Bus Transceiver***

The Bus Transceiver U3, a 74HC245, is used to allow the micro controller to read the front panel switches and the configuration dip switch. When the microcontroller desires to read the switches, pin 19 is asserted low and the switch data is placed on the data buss.

### ***Front Panel Switches***

The Front Panel Switches, SW1- SW4 are placed on data bits D0-D4 when the buss transceiver is enabled.

### ***Configuration Dip Switch***

Data bits D6 and D7 correspond to video format selection and test diagnostics enable.

### **Serial EEPROM**

The Non-volatile Memory, U6, a 93C46 Serial EEPROM, is used to store pattern selection and On Screen Display characters and position while power is removed from the generator. The Serial Bus is used to communicate to the EEPROM.

### **Micro Supervisor**

The microprocessor supervisor, U4, is a Maxim MAX699. This device asserts reset low if the supply voltage falls below 4.4 V. Once the supply recovers to above 4.65 volts reset is deasserted after 140 ms.

### **Serial Bus Communication**

The Serial Bus allows the microcontroller to communicate with the OSD and the Serial EEPROM. This is accomplished with the PB port of the microcontroller.

### **IIC Communication**

The (IIC) Bus is used to communicate with the Video Encoder. The same pins on the microcontroller are used for the IIC bus as with the serial bus.

### ***On Screen Display***

The On Screen Display (OSD),U11, is accomplished using a NEC uPD6453 On Screen Display IC. The timing control signals from the encoder are needed as well as the display clock, a derived clock, from the misc control EPLD, U12. For detail operation of the NEC OSD see the uPD6453 data sheet from NEC.

### ***Audio Oscillator***

The Audio Oscillator is a classic Wein bridge design with components selected for a frequency of 1kHz. The Wein bridge consists of an RC series network, R19 and C27, and an RC parallel network of R18 and C29. One half of U13 is the oscillator op amp and the other half is used as a peak detector to set the gain of the feed back stage with Q1. U17 is the output driver designed to drive a 600 ohm load with 0 dBu of audio. The output level is adjusted with R25 in the feed back path of one half of U17.

### ***Power Supply***

The power supply consists of a external 120 VAC to 9 VDC plug in transformer, TI, connected to power connector PS1. The main logic components are powered by +5V. D8 is a reverse current protection diode and provides some voltage drop to the linear regulator VR1. VR1 is a standard LM340 5 volt regulator. The negative supply for the audio section is generated by the Maxim switching regulator, U16, a MAX635.

# Replacement Parts List

## *Standard Board Parts List*

Table 3. Replacement Parts List

QTY	REFDES	PART NO.	DESCRIPTION	VALUE	PRICE EACH
26	C1, C2, C3, C4, C5, C6, C7, C8, C9, C11, C12, C14, C15, C16, C18, C20, C23, C24, C25, C26, C33, C34, C36, C39, C40, C41,	20-104	CAP MONO CERAMIC	0.1UF	\$0.38
2	C10, C55	25-224	CAP EL TANT 16V	2.2UF	\$0.44
3	C13, C17, C19,	25-226	CAP EL TANT 16V	22UF	\$1.49
2	C32, C43	25-475	CAP EL TANT 16V	47UF	\$3.12
3	C46, C47, C48	21-271	CAP MCER COG	270PF	\$0.36
3	C49, C50, C51	21-220	CAP MCER COG	22PF	\$0.36
3	C52, C53, C54	21-331	CAP MCER COG	330PF	\$0.36
3	L4, L5, L6	235-180	INDUCTOR	1.8UH	\$2.26
2	R1, R2	6-331-12	RES 1/4W 5%	330	\$0.05
5	R3, R4, R7, R22, R32	6-103-12	RES 1/4W 5%	10K	\$0.05
7	R5, R6, R8, R9, R10, R12, R14	6-510-12	RES 1/4W 5%	51	\$0.05
1	R24	6-111-12	RES 1/4W 5%	110	\$0.05
1	R36	6-471-12	RES 1/4W 5%	470	\$0.12
3	R30, R31, R37	6-7509-12	RES 1/4W 1%	75.0	\$0.12
1	R35	10-1000	RES VARIABLE	1K	\$2.79
1	D8	56-50	DIODE, POWER	1N4001	\$0.12

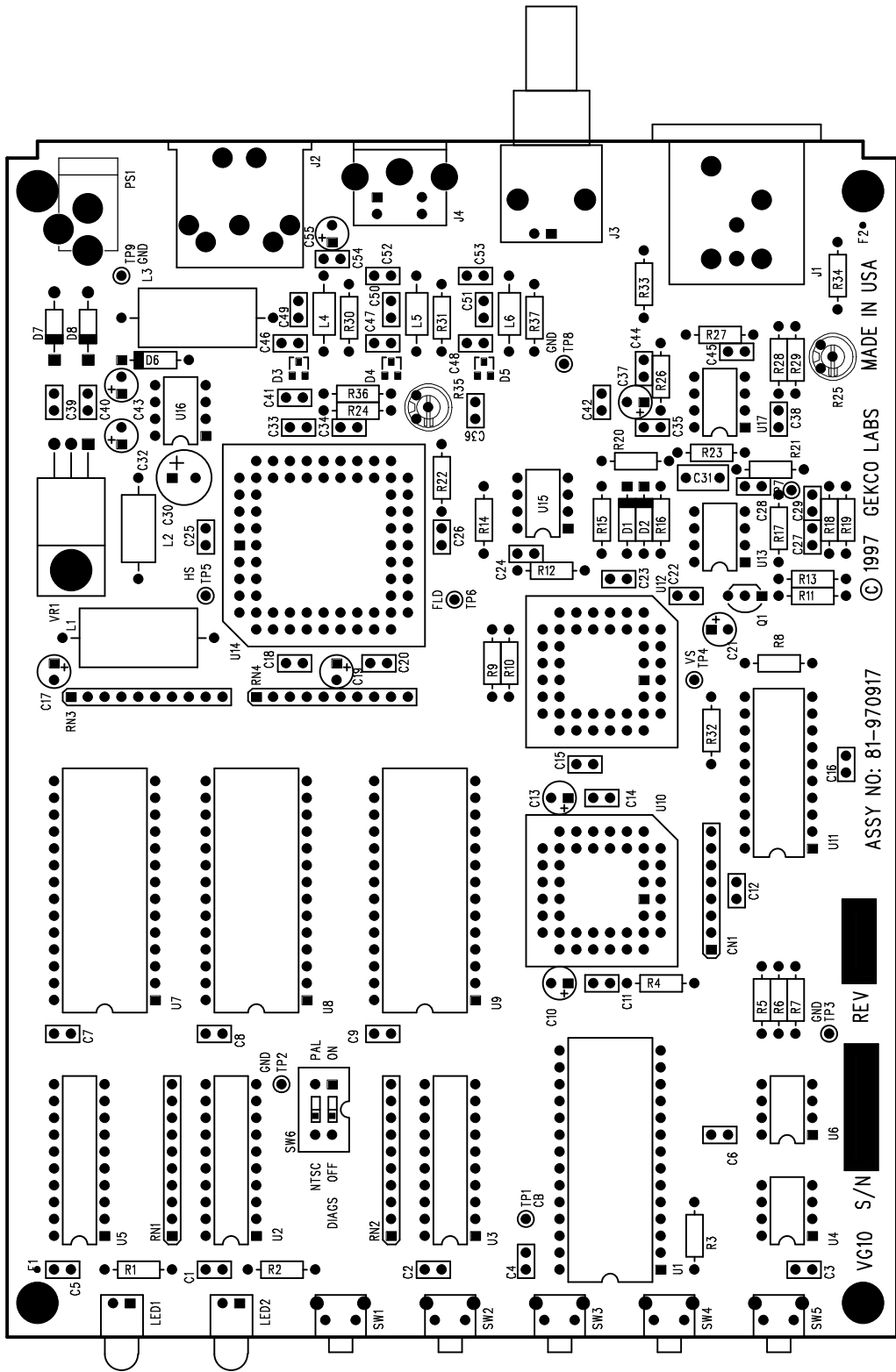
4	RN1, RN2, RN3, RN4	9-128	RESISTOR PACK 10 SIP	10K	\$0.43
1	J4	134-2240	CONN, SVHS	MINIDIN 4P	\$2.60
1	J3	134-1177	CONN. BNC		\$4.16
1	PS1	134-002	CONN. POWER, 2.1MM		\$0.38
1	VR1	442-54	IC, VOLTAGE REGULATOR 5V	LM340T-5	\$1.23
1		250-1411	SCREW 6-32x1/4"		\$0.04
1		252-3	NUT 6-32		\$0.02
1	L1	235-1000	INDUCTOR	10UH	\$1.88
1	X5	434-310	SOCKET IC	DIP20-300	\$0.28
2	X1, X9	434-312	SOCKET IC	DIP20-600	\$0.40
2	X10, X12	436-044	SOCKET PLCC 44P	PLCC44PSOC	\$3.96
1	X14	436-068	SOCKET PLCC 68P	PLCC68PSOC	\$4.30
2	LED1, LED2	412-256	LED CIRCUIT BRD	GREEN	\$0.70
5	SW1, SW2, SW3, SW4, SW5	64-1839	SWITCH MOMENTARY	SPDT	\$0.65
1	U5	444-245-01	IC EPLD, ADR. DECODER	GAL16V8	\$9.98
2	U2, U3	442-245	IC, BUS_XCVR	MC74HC245A	\$1.10
1	U1	444-000-01	IC, MCU 8BIT	MC68HC705P9	\$46.95
1	U4	442-699	IC, MICROSUPERVISOR	MAX699CPA	\$8.37
1	U9	442-064	IC STATIC RAM 8KX8	6264-70	\$4.18
1	U10	444-952-01	IC PROG. LOGIC	ADRCTRL1	\$15.00
1	U12	444-953-01	IC PROG. LOGIC	MEMCTRL1	\$15.00
1	U14	442-866	IC, VIDEO ENCODER	BT866KPJ	\$22.00
1	U15	442-1817	IC, OSC27MHZ		\$7.10
1	T1	54-103	XFRMR PLUG IN 120 VAC TO 9 VDC@500MA		\$10.00
1		81-970730	PCB MAIN BOARD		\$49.00
1		595-321	ASSEMBLY MANUAL		\$10.00
1		595-322	OPERATION/SERVICE MANUAL		\$10.00

Standard Patterns		STD Option 1			
QTY	REFDES	PART NO.	DESCRIPTION	VALUE	PRICE EACH
1	U1	444-1XX-01	IC MICRO, MCU 8BIT	MC68HC705P9	\$49.00
1	U9	442-256	STATIC RAM 32KX8	MS62256-70	\$6.45
1	U6	442-9346	IC, SERIAL PROM	93C46	\$2.77
Enhanced Patterns		Option 2			
1	U1	444-X2X-01	IC, MCU, 8BIT	MC68HC705P9	\$46.95
1	U7	444-344-01	Y PATTERN EPROM 32KX8	27HC256-70	\$17.90
1	U8	444-345-01	UV PATTERN EPROM 32KX8	27HC256-70	\$17.90
2	X7, X8	434-312	SOCKET IC DIP28-600		\$0.40

On Screen Display		Option 3			
1	U1	444-XX3-01	IC, MCU 8BIT	MC68HC705P6	\$59.00
1	U11	442-6543	IC, ON SCREEN DISPLAY	UPD6543CY-001	\$19.19
1	J2	132-2350	CONNECTOR, KEYBOARD	DIN5PS	\$0.92
Audio Oscillator		Option 4			
QTY	REFDES	PART NO.	DESCRIPTION	VALUE	PRICE EACH
5	C22, C28, C35, C42, C45	20-104	CAP MONO CERAMIC, 50V	0.1UF	\$0.38
1	C37	25-226	CAP EL TANT 16V	22UF	\$0.73
1	C21	25-225	CAP EL TANT 16V	10UF	\$1.99
2	C27, C29	21-102	CAP MONO CERAMIC 100V	1000PF	\$0.42
1	C30	26-102	CAP EL ALUM 16V	100UF	\$1.88
1	C31	23-105	CAP MONO CERAMIC 50V	1UF	\$2.36
1	L3	236-330	INDUCTOR	330UH	\$5.64
3	D1, D2, D6	56-56	DIODE SIGNAL	1N4148	\$1.12
1	R15	6-2001-12	RES 1/4W 1%	2.0K	\$0.12
2	R16, R17	6-2002-12	RES 1/4W 1%	20K	\$0.12
2	R18, R19	6-2002-12	RES 1/4W 1%	158K	\$0.12
1	R11	6-9531-12	RES 1/4W 1%	9.53K	\$0.12
1	R13	6-433-12	RES 1/4W 5%	43K	\$0.12
1	R20	6-6811-12	RES 1/4W 1%	6.81K	\$0.12
3	R21, R23, R26	6-103-12	RES 1/4W 5%	10K	\$0.12
2	R27, R28	6-4991-12	RES 1/4W 1%	4.99K	\$0.12
1	R29	6-3011-12	RES 1/4W 1%	3.01K	\$0.12
2	R33, R34	6-2490-12	RES 1/4W 1%	24.9	\$0.12
2	C38, C44	21-560	CAP MONO CER COG	56PF	\$0.36
1	Q1	417-5457	TRANSISTOR, NJFET	2N5457	\$2.62
1	R25	10-203	RES VARIABLE	20K	\$3.81
1	U16	442-635	DCTODC_CONV MAX635	MAX635	\$11.20
1	U13	442-062	OP AMP TL062	TL062N	\$2.12
1	U17	442-833	OP AMP LM833	LM833N	\$3.96
1	J1	134-568	CONNECTOR, PC XLR MALE		\$3.25
		Option 5			
1		85-19216	ENCLOSURE		\$49.00

## Circuit Board Assembly Drawing

*Figure 4. Assembly Drawing*



ASSY NO: 81-970917

REV [REDACTED]

VG10 S/N [REDACTED]

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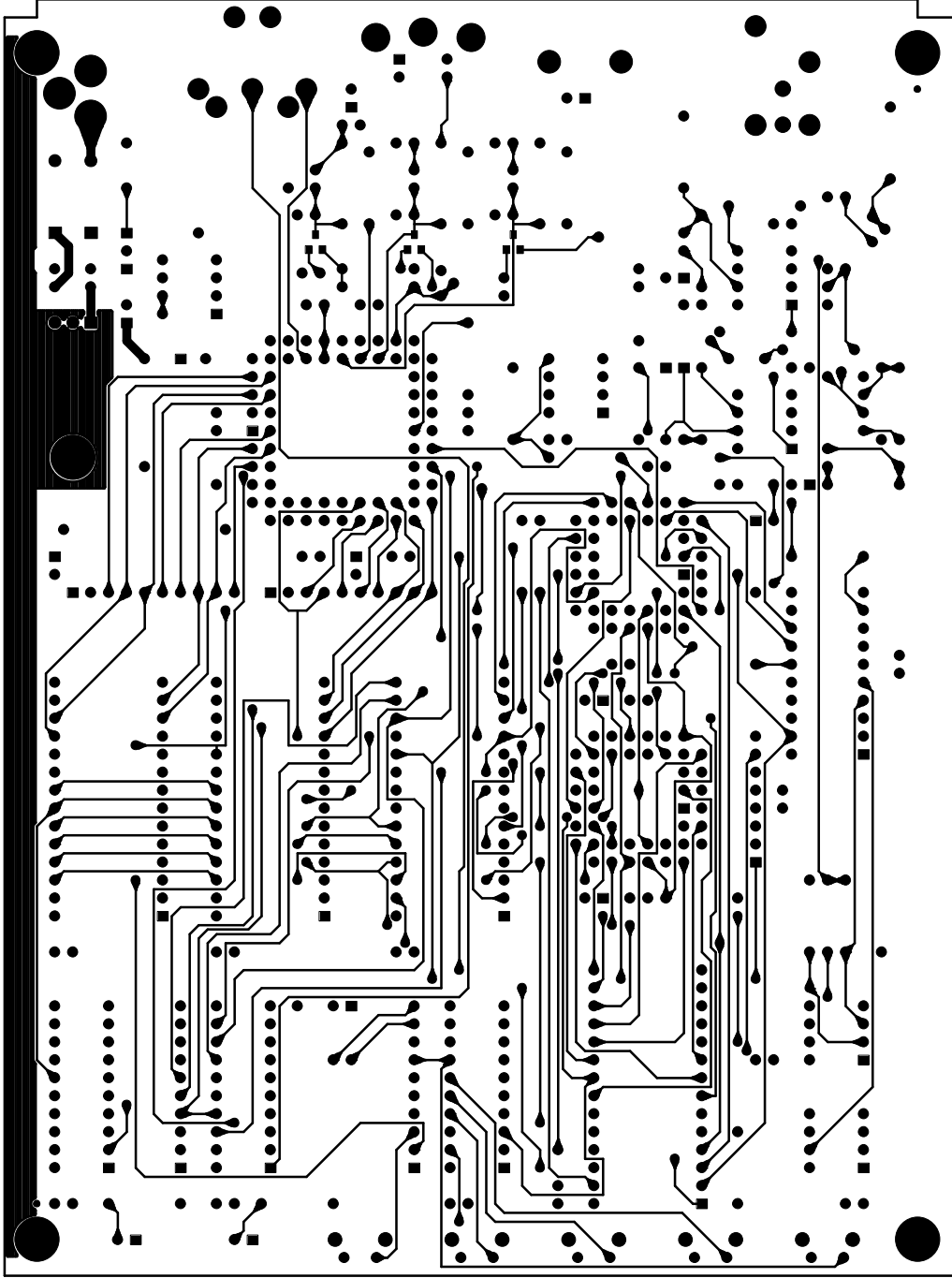
MADE IN USA

F2

## Circuit Board X-RAY Views

*Figure 5. Layer 1 Top Signals*





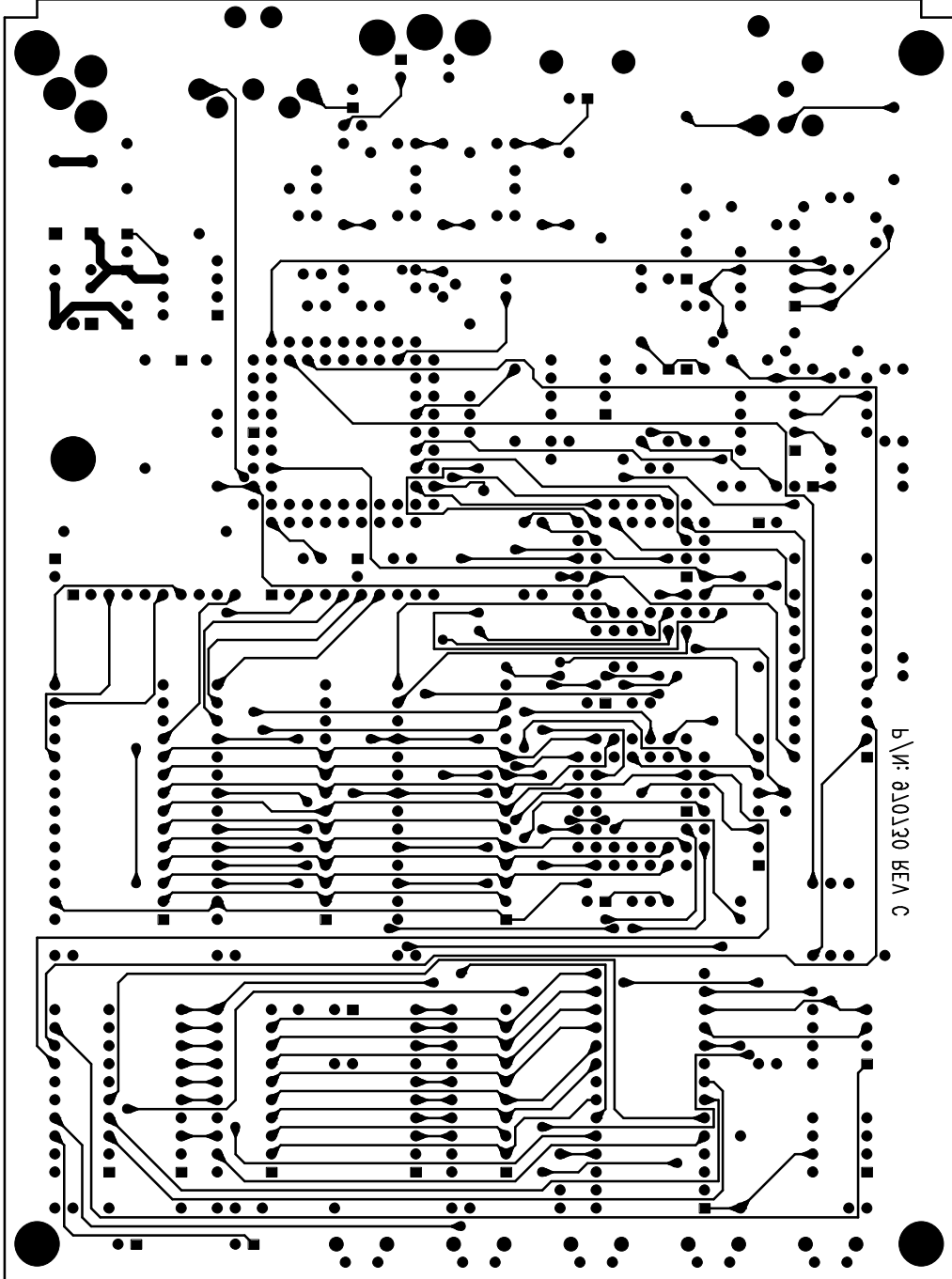
LAYER 1 (TOP SIDE)

L1:PHO

*Figure 6. Layer 2 Ground Plane*

*Figure 7. Layer 3 Power Plane*

*Figure 8. Layer 4 Bottom Signals*



b/w: 010130 REV C

LAYER 4 (BOTTOM SIDE) L4.PHO

# Appendix A

## Test Pattern Specifications

### Standard Patterns

### SMPTE Color Bars

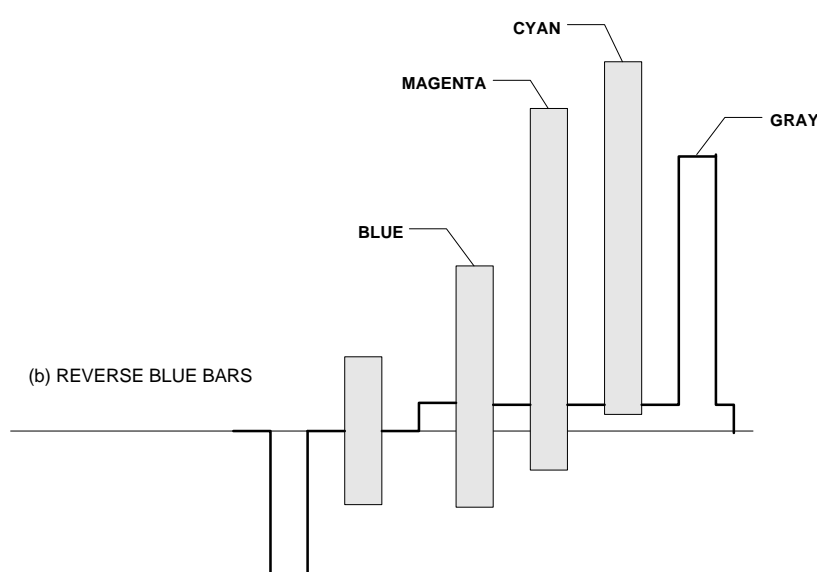
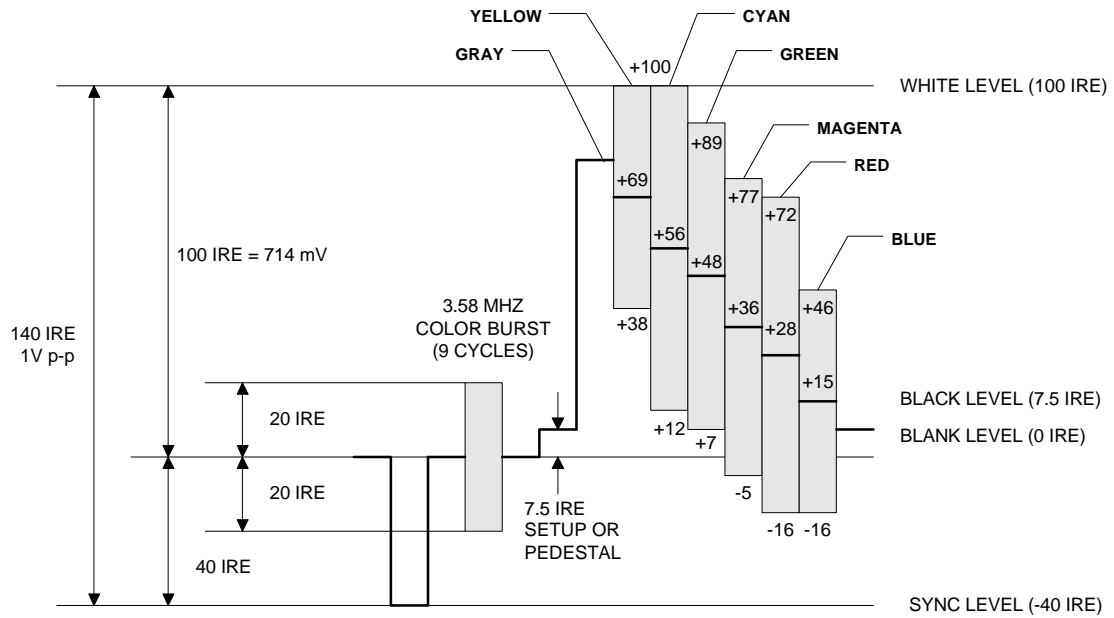


Figure 9. SMPTE Color Bars

**Color Black**

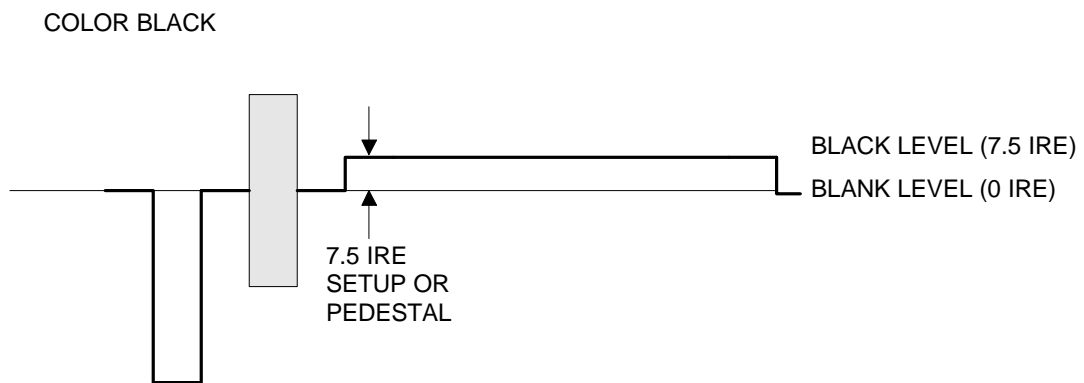
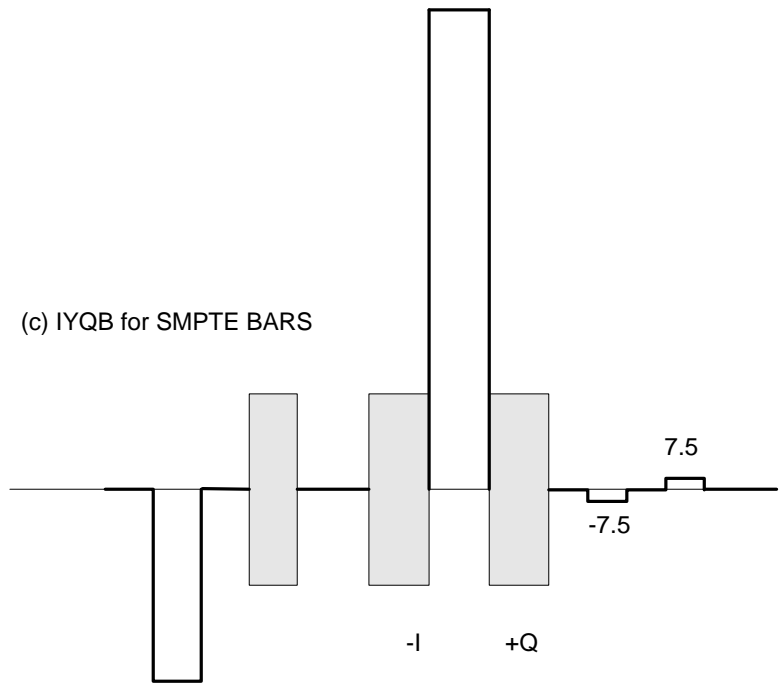


Figure 10. Color Black

## Schematics

*Top Block Diagram Sheet 1*



***Microcontroller***

***Sheet 2***

***SRAM Memory***

***Sheet 3***

***EPROM Memory***      ***Sheet 4***

***Address Control      Sheet 5***

***Video Encoder***

***Sheet 6***

***On Screen Display Sheet 7***

***Audio Oscillator***      ***Sheet 8***

***Power Supply***

***Sheet 9***



***Decoupling Capacitors Sheet 10***

***Decoupling Capacitors Sheet 11***

# Warranty

## YOUR GEKCO FACTORY ASSEMBLED PRODUCT

### ONE YEAR LIMITED WARRANTY

Welcome to GEKCO products. We believe you will be pleased with the performance of your product. Please read this consumer protection plan carefully. It is a "LIMITED WARRANTY" as defined in the U.S. Consumer Product Warranty and Federal Trade Commission Improvement Act. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

### GEKCO'S RESPONSIBILITY

**PARTS** - Replacement for factory defective parts will be supplied free for one year from date of purchase. Replacement parts are warranted for the remaining portion of the original warranty period. You can obtain warranty parts direct from GEKCO by writing or telephoning us at (425) 392-0638. We will pay the shipping charges to get those parts to you.... anywhere in the world.

**SERVICE LABOR** - For a period of one year from the date of purchase, any malfunction caused by factory defective parts or workmanship will be corrected at no charge to you. You must deliver the unit at your expense to GEKCO.

**TECHNICAL CONSULTATION** - You will receive free consultation on any problem you might encounter in the use of your GEKCO product. Just drop us a line or give us a call. Sorry, we cannot accept collect calls.

**NOT COVERED** - Repair service, adjustments and calibrations due to misuse, abuse or negligence are not covered by this warranty. Unauthorized modification of the product or of any furnished component will void this warranty in its entirety. This warranty does not include reimbursement for inconvenience, installation, set-up time, lost of use, or unauthorized service.

This warranty covers only GEKCO factory assembled products and is not extended to other equipment and components that a customer uses in conjunction with our products.

SUCH REPAIR AND/OR PARTS REPLACEMENT SHALL BE THE SOLE REMEDY OF THE CUSTOMER AND THERE SHALL BE NO LIABILITY ON THE PART OF GEKCO FOR ANY SPECIAL, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOSS OF BUSINESS OR PROFITS, WHETHER OR NOT FORESEEABLE.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

### OWNERS RESPONSIBILITY

**EFFECTIVE WARRANTY DATE** - Warranty begins on the date of first consumer purchase. You must supply a copy of your proof of purchase when you request warranty service or parts.

**OPERATING MANUAL** - Read your operating instructions carefully so that you will fully understand the proper operation and function of your unit.

**ACCESSORY EQUIPMENT** - Performance malfunctions involving connections to (or interfacing with) other non-GEKCO equipment are not covered by this warranty and are the owner's responsibility.

**SHIPPING UNITS** - Follow the packing instructions published in your manual. Damage due to inadequate packing can not be repaired under warranty.

If you are not satisfied with our service (warranty or otherwise) or our products, write directly to GEKCO, CUSTOMER SERVICE, PO Box 642, Issaquah WA 98027. We will make certain your problems receive immediate, personal attention.

GEKCO reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.